L2106S

Half-Bridge Driver

1. Description

The L2106S is a high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

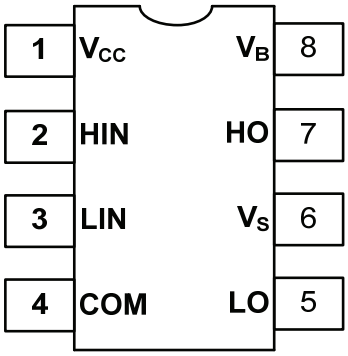
2. Features

- Floating channel designed for bootstrap operation to + 600 V
- Gate driver supply range from 10 to 20 V
- Under-voltage lockout
- 3.3V, 5 V and 15 V logic compatible
- Matched propagation delay for both channels
- Internal minimum set dead-time
- High side output in phase with HIN input
- Low side output out of phase with LIN input
- LEAD-FREE (ROHS Compliant)

3. Applications

- Motor driver e-bike R.C., ballast, power audio amplifier

4. Pin Assignments



SOP-8L

5. Marking Information

Product Name	Marking	
L2106S	L2106S XXXXX	X : Date Code

6. Ordering Code

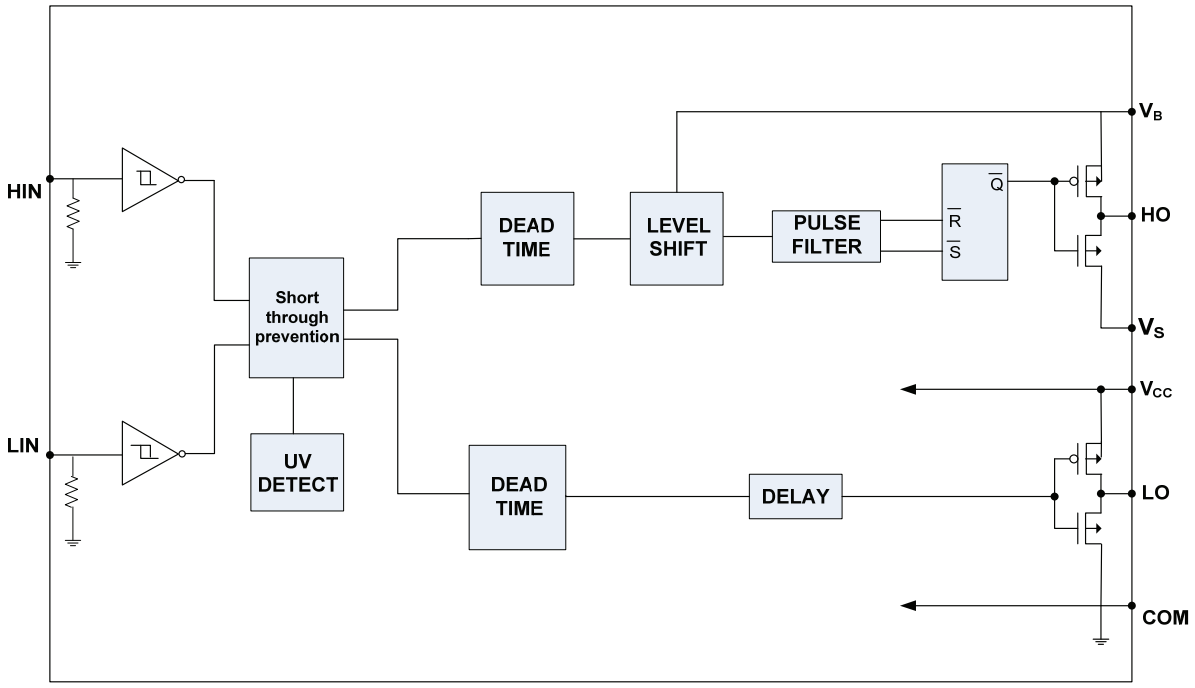
L2106S └— Assembly Material	Assembly Material G: Halogen and Lead Free Device

Note: LUL defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

7. Pin Definitions

Pin No.	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output
3	LIN	Logic input for low side gate driver output
4	COM	Low side return
5	LO	Low side gate driver output
6	V_S	High side floating supply return
7	HO	High side gate driver
8	V_B	High side floating supply

8. Block Diagram



9. Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	600	V
V_S	High side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	- 0.3	20	
V_{LO}	Low side output voltage	- 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	- 0.3	V_{CC} + 0.3	
dV_S / dt	Allowable offset supply voltage transient	—	50	V / ns
P_D	Package power dissipation @ $T_A \leq +25\ ^oC$	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	^oC / W
T_J	Junction temperature	- 40	150	^oC
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

10. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_B	High side floating supply absolute voltage		V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	$V_{BS} \geqq 12V$	- 6	600	
		$V_{BS} < 12V$	$- V_{BS} / 2$		
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage		10	20	
V_{LO}	Low side output voltage		0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)		0	V_{CC}	
T_A	Ambient temperature		- 40	125	^oC

11. Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, T_A = 25 ºC unless otherwise specified. The V_{IN}, $V_{TH\ and}$ I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Logic " 1 " input voltage	V_{CC} = 10 V to 20 V	3	-	-	V
V_{IL}	Logic " 0 " input voltage	V_{CC} = 10 V to 20 V	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	-	-	100	mV
V_{OL}	Low level output voltage		-	-	100	
I_{LK}	Offset supply leakage current	V_B = V_S = 500 V	-	-	60	uA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	-	25	-	
I_{QCC}	Quiescent V_{CC} supply current	V_{IN} = 0 V or 5 V	-	300	-	
I_{IN+}	Logic " 1 " input bias current	V_{IN} = 5 V	-	5	15	
I_{IN-}	Logic " 0 " input bias current	V_{IN} = 0 V	-	-	15	
V_{CCUV+}	V_{CC} supply under voltage positive going threshold		7.8	8.8	9.8	V
V_{CCUV-}	V_{CC} supply under voltage negative going threshold		7	8.0	9.0	
I_{O+}	Souring current		-	250	-	mA
I_{O-}	Sink current		-	320	-	mA

12. Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25 ºC unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	-	1000	-	ns	VS = 0 V
t_{off}	Turn-off propagation delay	-	500	-		VS = 0 V or 600V
t_r	Turn-on rise time	-	100	-		
t_f	Turn-off fall time	-	50	-		VS = 0 V
MT	Delay matching | t_{on} – t_{off} |	-	-	50		
DT	Dead-time : LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	-	560	-		

Note：1. PWM pulse width must be ≧ 1 μsec

13. Timing Diagram

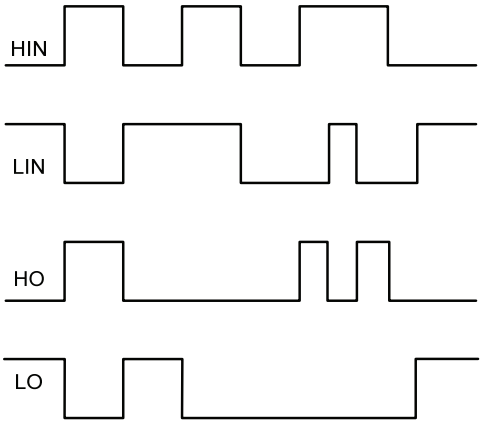


Figure 1. Input / Output Timing Diagram

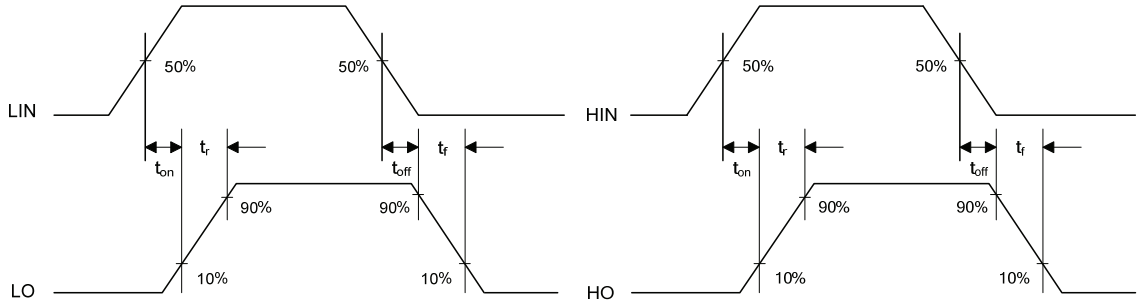


Figure 2. Switching Time Waveform Definition

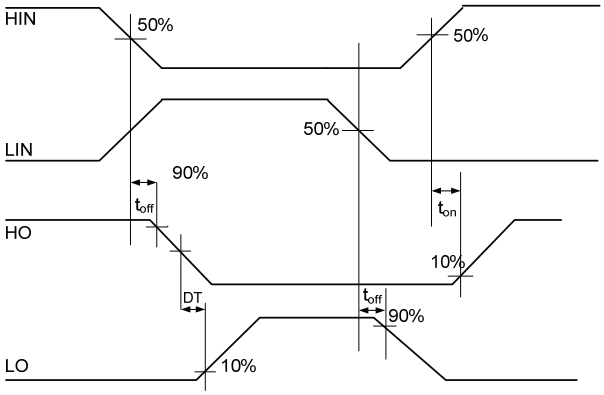
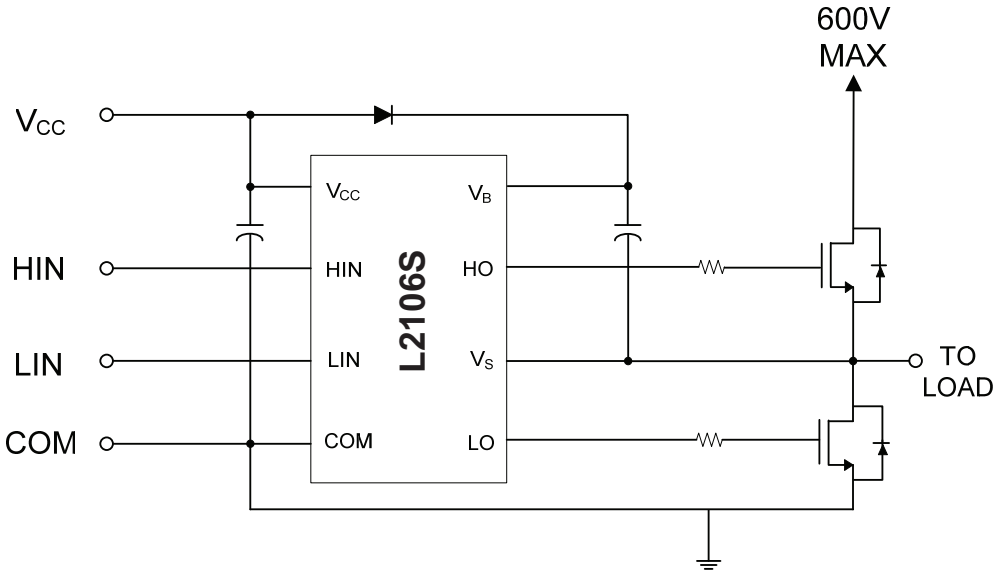


Figure 3. Dead-Time Waveform Definition

14. Application Circuit



15. Package Dimensions

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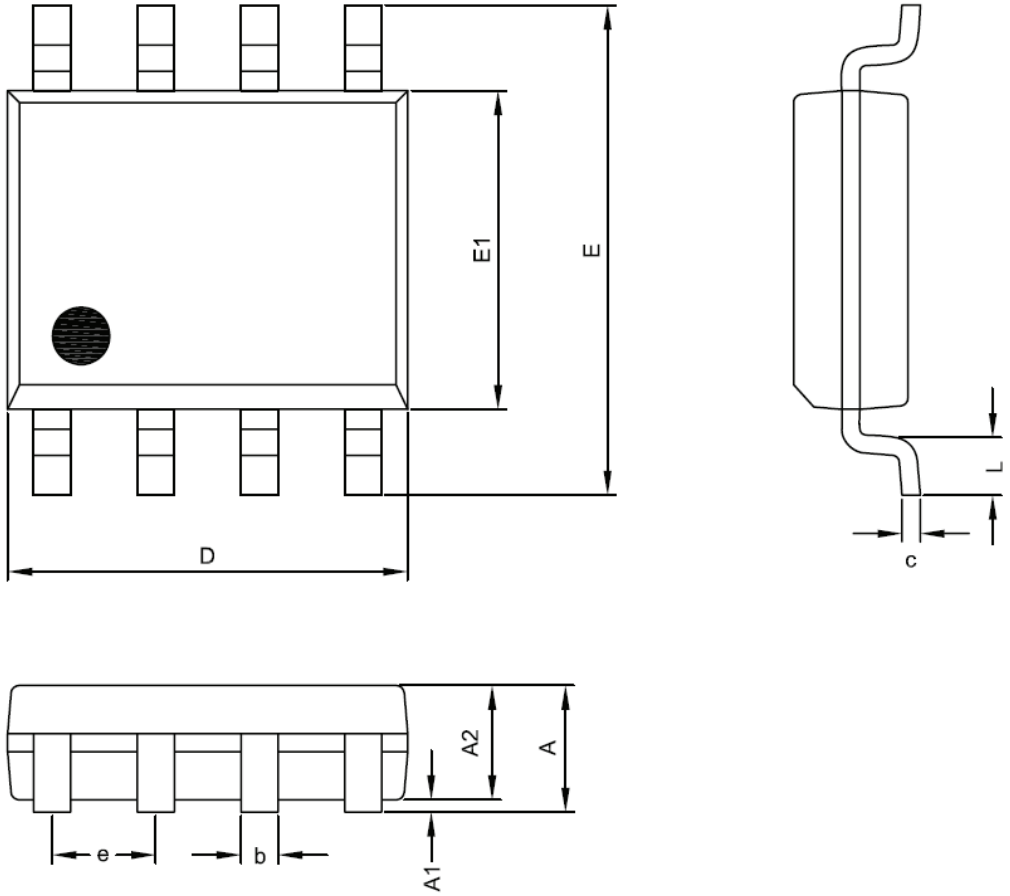

Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. JEDEC outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.