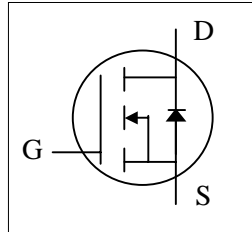
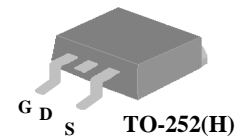




- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	500V
$R_{DS(ON)}$	1.4 $\Omega$
$I_D$	5.0A



## Description

The AP05N50 provide high blocking voltage to overcome voltage surge and sag in the toughest power system with the best combination of fast switching, ruggedized design and cost-effectiveness.

The TO-252 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications.

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	500	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V	5.0	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V	2.8	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	18	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	73.5	W
	Linear Derating Factor	0.59	W/ $^\circ C$
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	2	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>	45	mJ
$I_{AR}$	Avalanche Current	3	A
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

## Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	1.7	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) <sup>4</sup>	62.5	$^\circ C/W$



**Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	500	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>3</sup>	$V_{GS}=10V, I_D=2.7A$	-	-	1.4	$\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=2.7A$	-	2.4	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=500V, V_{GS}=0V$	-	-	25	$\mu A$
	Drain-Source Leakage Current ( $T_j=125^{\circ}\text{C}$ )	$V_{DS}=400V, V_{GS}=0V$	-	-	250	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>3</sup>	$I_D=3.1A$ $V_{DS}=400V$ $V_{GS}=10V$	-	19	30	nC
$Q_{gs}$	Gate-Source Charge		-	4.6	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge		-	6.3	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>3</sup>	$V_{DD}=250V$ $I_D=3.1A$	-	11	-	ns
$t_r$	Rise Time		-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=12\Omega, V_{GS}=10V$ $R_D=80.6\Omega$	-	32	-	ns
$t_f$	Fall Time		-	10	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$	-	985	1580	pF
$C_{oss}$	Output Capacitance		-	85	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3.3	-	pF
$R_g$	Gate Resistance	$f=1.0MHz$	-	2.5	3.8	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>3</sup>	$T_j=25^{\circ}\text{C}, I_S=4.5A, V_{GS}=0V$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time <sup>3</sup>	$I_S=3.1A, V_{GS}=0V,$ $di/dt=100A/\mu s$	-	300	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	2.6	-	$\mu C$

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Starting  $T_j=25^{\circ}\text{C}$  ,  $V_{DD}=50V$  ,  $L=10mH$  ,  $R_G=25\Omega$  ,  $I_{AS}=3A$ .
- 3.Pulse test
- 4.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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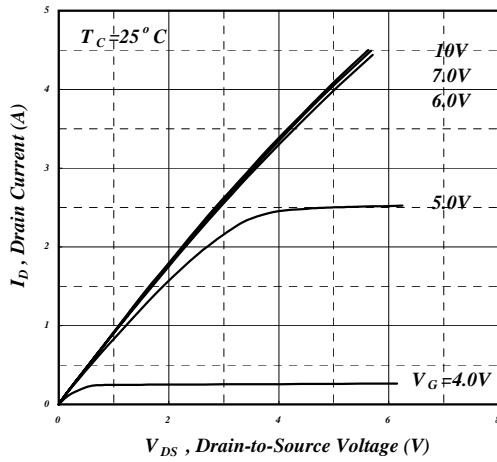


Fig 1. Typical Output Characteristics

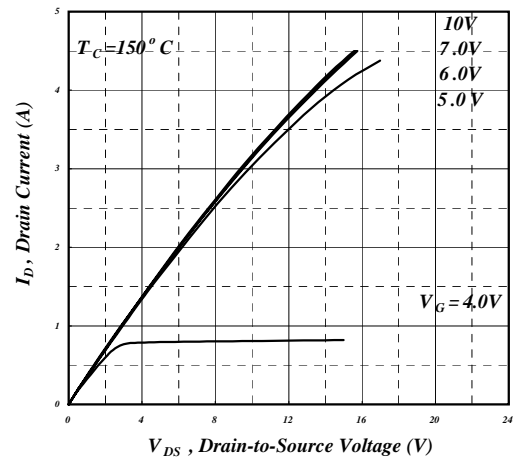


Fig 2. Typical Output Characteristics

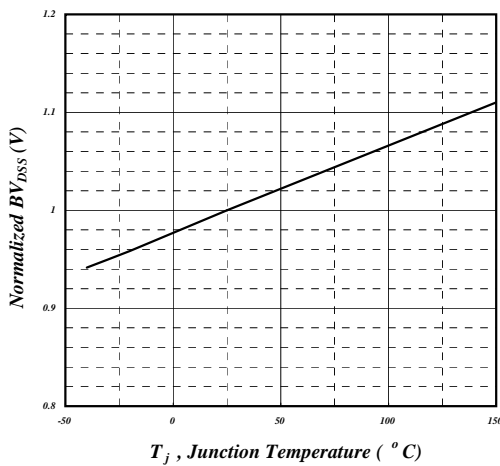


Fig 3. Normalized  $BV_{DSS}$  v.s. Junction Temperature

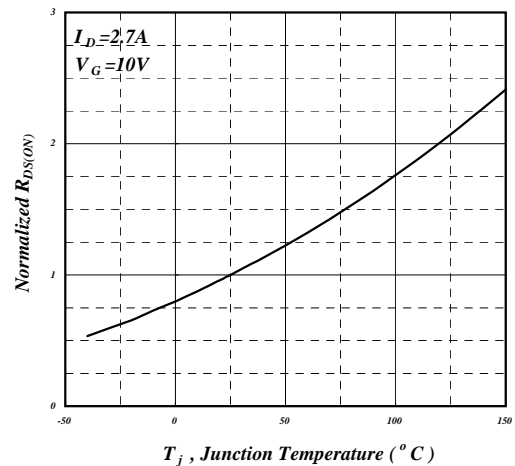


Fig 4. Normalized On-Resistance v.s. Junction Temperature

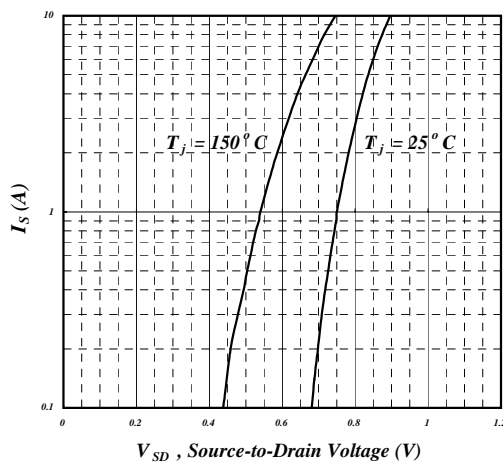


Fig 5. Forward Characteristic of Reverse Diode

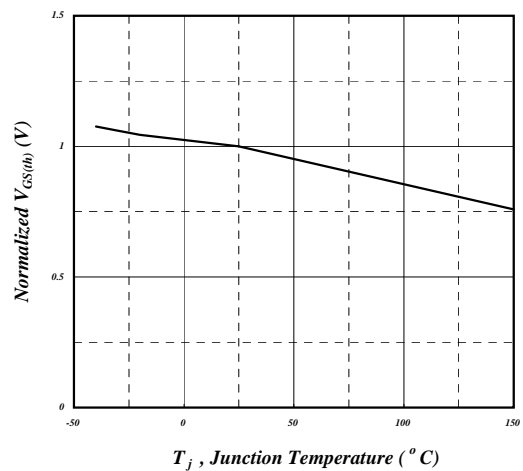


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

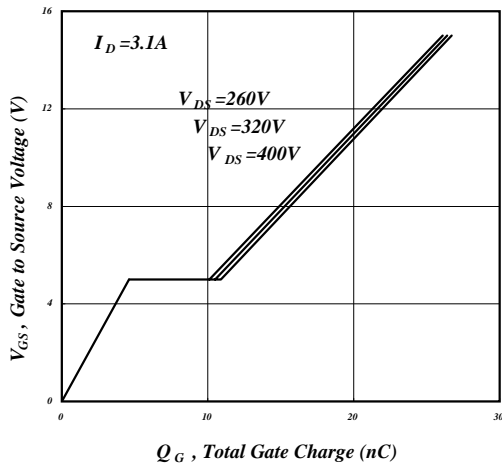


Fig 7. Gate Charge Characteristics

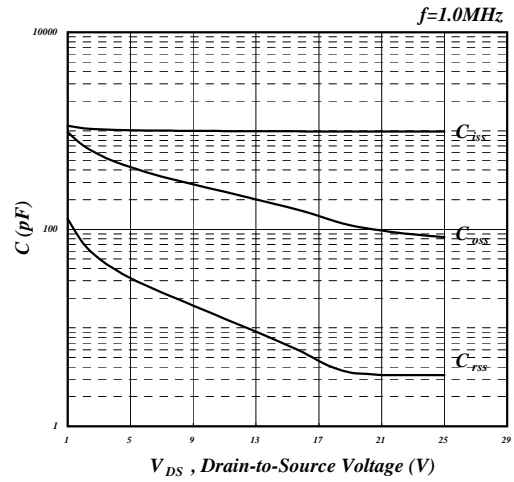


Fig 8. Typical Capacitance Characteristics

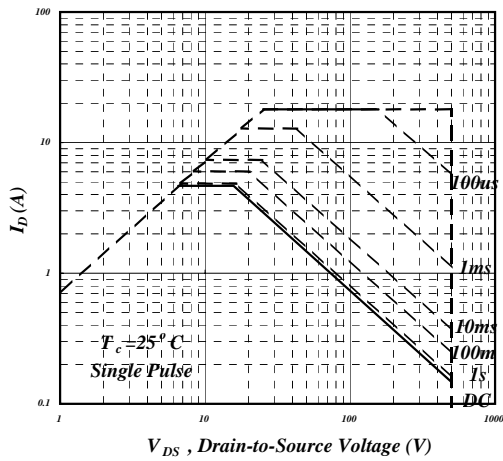


Fig 9. Maximum Safe Operating Area

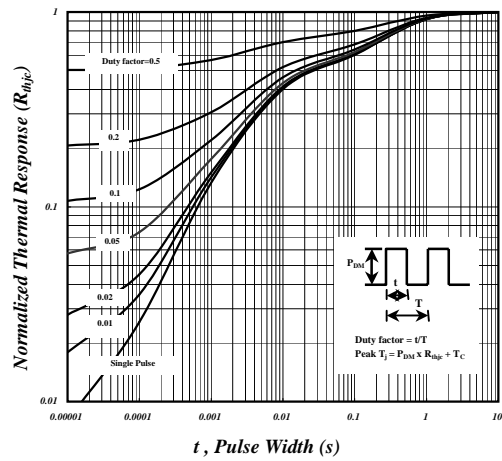


Fig 10. Effective Transient Thermal Impedance



Fig 11. Switching Time Waveform

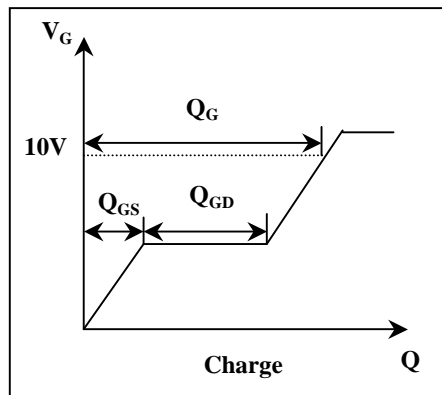


Fig 12. Gate Charge Waveform